REMARKS

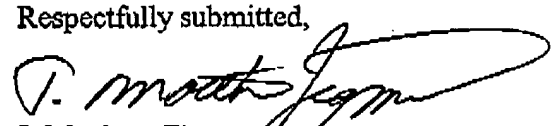
After entry of this amendment claims 3-6, 17-21, 23-25, and 27-30 will remain pending in this application. Claims 1, 2, 16, 22, and 26 have been canceled without prejudice.

Claims 3, 6, 17, 23-25, and 27 have been indicated as being allowable. Accordingly, claims 3, 6, 17, 23, 25, and 27 have been rewritten as independent. Claims 4, 18, and 28 have been amended to change dependency. Claims 24 and 25 have been amended for consistency. No new matter has been added. Applicants submit that this amendment does not raise any new issues for consideration.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance and an action to that end is urged. If the Examiner believes a telephone conference would aid in the prosecution of this case in any way, please call the undersigned at 650-752-2456.

Respectfully submitted,



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3. (Amended) **[The method of claim 2]** A method of buffering an input signal comprising:

receiving the input signal, wherein the input signal alternates between a first polarity and a second polarity;

generating a first current, wherein the first current is proportional to the input signal when the input signal has the first polarity, and approximately equal to zero when the input signal has the second polarity;

generating a second current, wherein the second current is proportional to the input signal when the input signal has the second polarity, and approximately equal to zero when the input signal has the first polarity;

generating a third current proportional to the first current;

generating a fourth current proportional to the second current;

applying the first and fourth currents to a first terminal of an inductor; and

applying the second and third currents to a second terminal of the inductor,

wherein a capacitance is between the first terminal of the inductor and the second terminal of the inductor, and the inductor and capacitance form a tank circuit, and

wherein the input signal alternates between the first polarity and the second polarity at a first frequency, the tank circuit has a resonant frequency of a second frequency, and the first frequency and second frequency are approximately equal.

4. (Amended) The method of claim [2] 3 wherein the first current and the second current are generated by NMOS devices.

6. (Amended) **[The method of claim 2]** A method of buffering an input signal comprising:

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receiving the input signal, wherein the input signal alternates between a first polarity and a second polarity;

generating a first current, wherein the first current is proportional to the input signal when the input signal has the first polarity, and approximately equal to zero when the input signal has the second polarity;

generating a second current, wherein the second current is proportional to the input signal when the input signal has the second polarity, and approximately equal to zero when the input signal has the first polarity;

generating a third current proportional to the first current;

generating a fourth current proportional to the second current;

applying the first and fourth currents to a first terminal of an inductor; and

applying the second and third currents to a second terminal of the inductor,

wherein a capacitance is between the first terminal of the inductor and the second terminal of the inductor, and the inductor and capacitance form a tank circuit, and

wherein the first current is geometrically proportional to the input signal when the input signal has the first polarity, and the second current is geometrically proportional to the input signal when the input signal has the second polarity.

17. (Amended) **[The circuit of claim 16 further comprising:]** A circuit for buffering RF signals comprising:

a first device coupled between a first output node and a first supply node, having a control electrode coupled to a first input node;

a second device coupled between a second output node and the first supply node, having a control electrode coupled to a second input node;

a third device coupled between a second supply node and the first output node, having a control electrode coupled to the second output node;

a fourth device coupled between the second supply node and the second output node, having a control electrode coupled to the first output node;

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a fifth device coupled between the first device and the first output node;

[and]

a sixth device coupled between the second device and the second output node; and

an inductor coupled between the first output node and the second output node.

18. (Amended) The circuit of claim **[16]** 17 wherein the first device and the second device are NMOS devices, and the third device and fourth device are PMOS devices.

23. (Amended) **[The method of claim 22]** A method of buffering an RF signal comprising:

receiving the RF signal, wherein the RF signal alternates between a first polarity and a second polarity;

generating a first current, wherein the first current is proportional to the RF signal when the RF signal has the first polarity, and approximately equal to zero when the RF signal has the second polarity;

generating a second current, wherein the second current is proportional to the RF signal when the RF signal has the second polarity, and approximately equal to zero when the RF signal has the first polarity;

using the first current to generate a third current, the third current proportional to the first current;

using the second current to generate a fourth current, the fourth current proportional to the second current;

applying the first and fourth currents to a first terminal of an inductor; and

applying the second and third currents to a second terminal of the inductor,

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wherein a capacitance is coupled between the first terminal of the inductor and the second terminal of the inductor, and the inductor and capacitance form a tank circuit.

24. (Amended) The method of claim 23 wherein the **[input]** RF signal alternates between the first polarity and the second polarity at a first frequency, the tank circuit has a resonant frequency of a second frequency, and the first frequency and second frequency are approximately equal.

25. (Amended) **[The method of claim 22]** A method of buffering an RF signal comprising:

receiving the RF signal, wherein the RF signal alternates between a first polarity and a second polarity;

generating a first current, wherein the first current is proportional to the RF signal when the RF signal has the first polarity, and approximately equal to zero when the RF signal has the second polarity;

generating a second current, wherein the second current is proportional to the RF signal when the RF signal has the second polarity, and approximately equal to zero when the RF signal has the first polarity;

using the first current to generate a third current, the third current proportional to the first current;

using the second current to generate a fourth current, the fourth current proportional to the second current;

applying the first and fourth currents to a first terminal of an inductor; and

applying the second and third currents to a second terminal of the inductor,

wherein the first current is geometrically proportional to the **[input]** RF signal when the **[input]** RF signal has the first polarity, and the second current is geometrically proportional to the **[input]** RF signal when the **[input]** RF signal has the second polarity.

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27. (Amended) **[The circuit of claim 26 further comprising:]** An RF amplifier comprising:

a first device coupled between a first output node and a first supply node, having a control electrode configured to receive an RF signal, and further configured to operate near cutoff in the absence of the RF signal;

a second device coupled between a second output node and the first supply node, having a control electrode configured to receive a complement of the RF signal, and further configured to operate near cutoff in the absence of the complement of the RF signal;

a third device coupled between a second supply node and the first output node, having a control electrode coupled to the second output node;

a fourth device coupled between the second supply node and the second output node, having a control electrode coupled to the first output node;

a fifth device coupled between the first device and the first output node; **[and]**

a sixth device coupled between the second device and the second output node; and

an inductor coupled between the first output node and the second output node.

28. (Amended) The circuit of claim **[26]** 27 wherein the first device and the second device are NMOS devices, and the third device and fourth device are PMOS devices.

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